SCANNED, # 12

Fig. 1

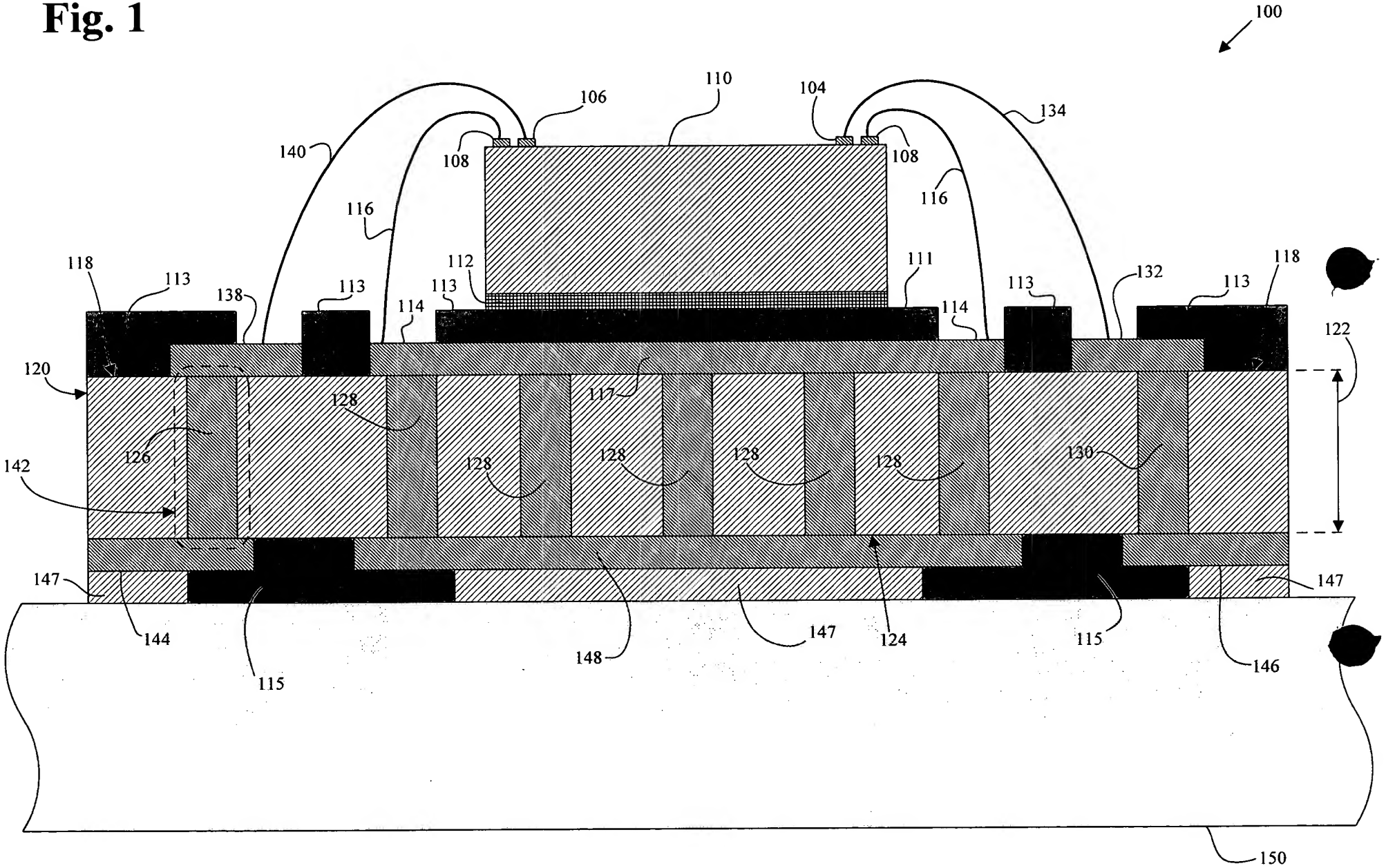
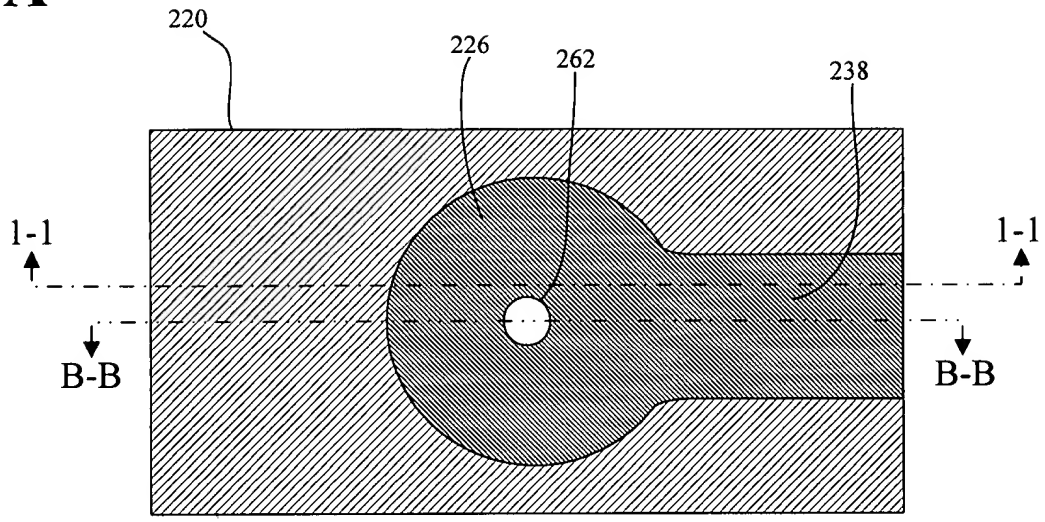


Fig. 2A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262
238
1-1
1-1
B-B
B-B

Fig. 2B

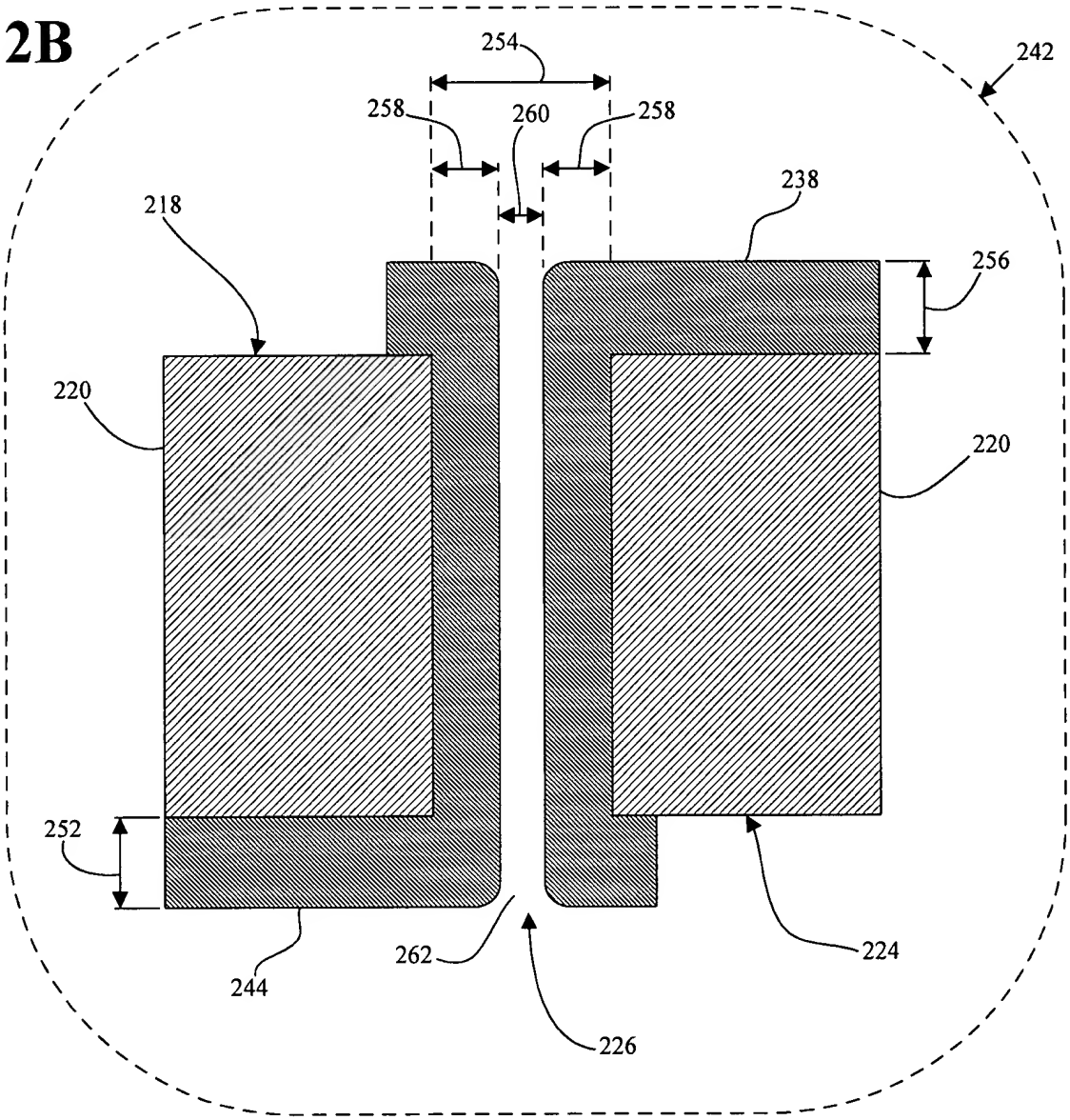
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Fig. 3

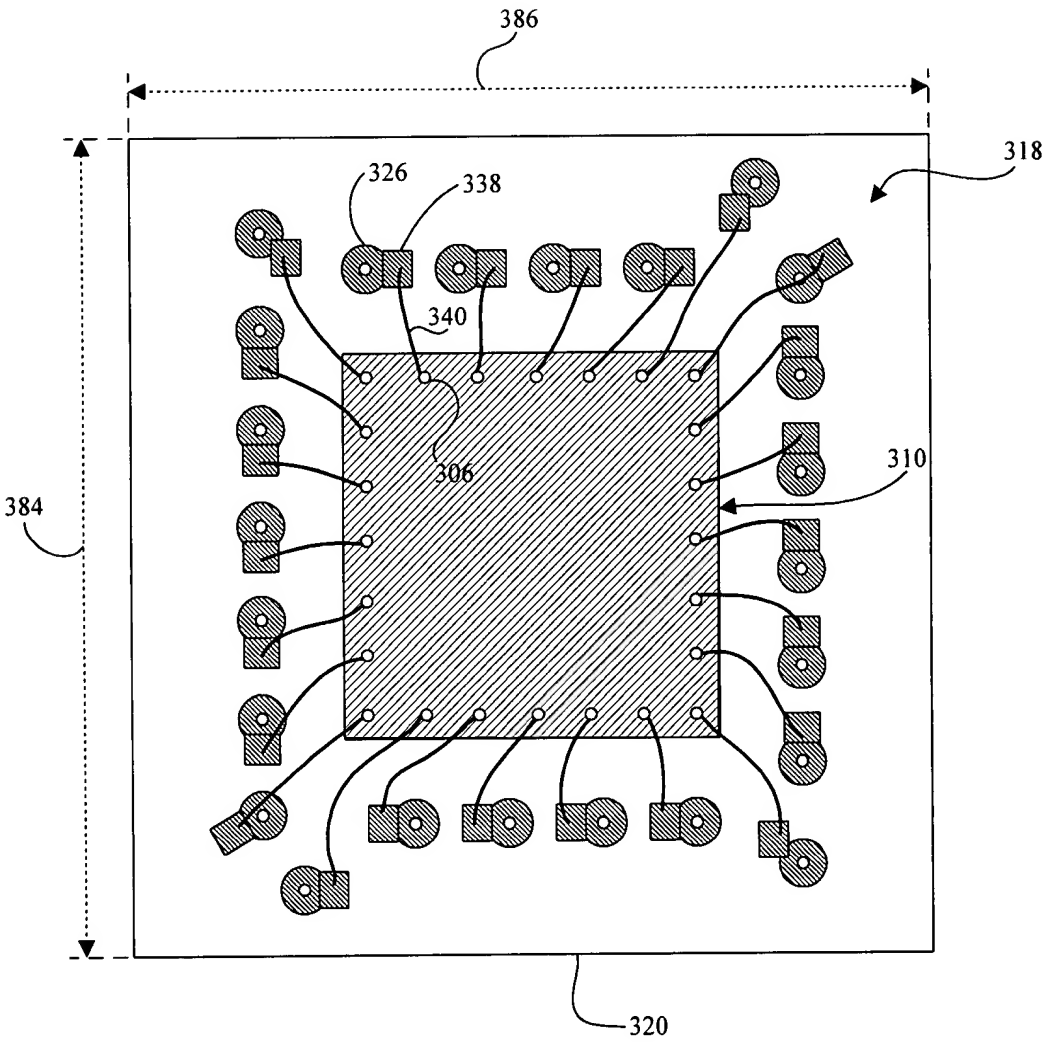

Fig. 4

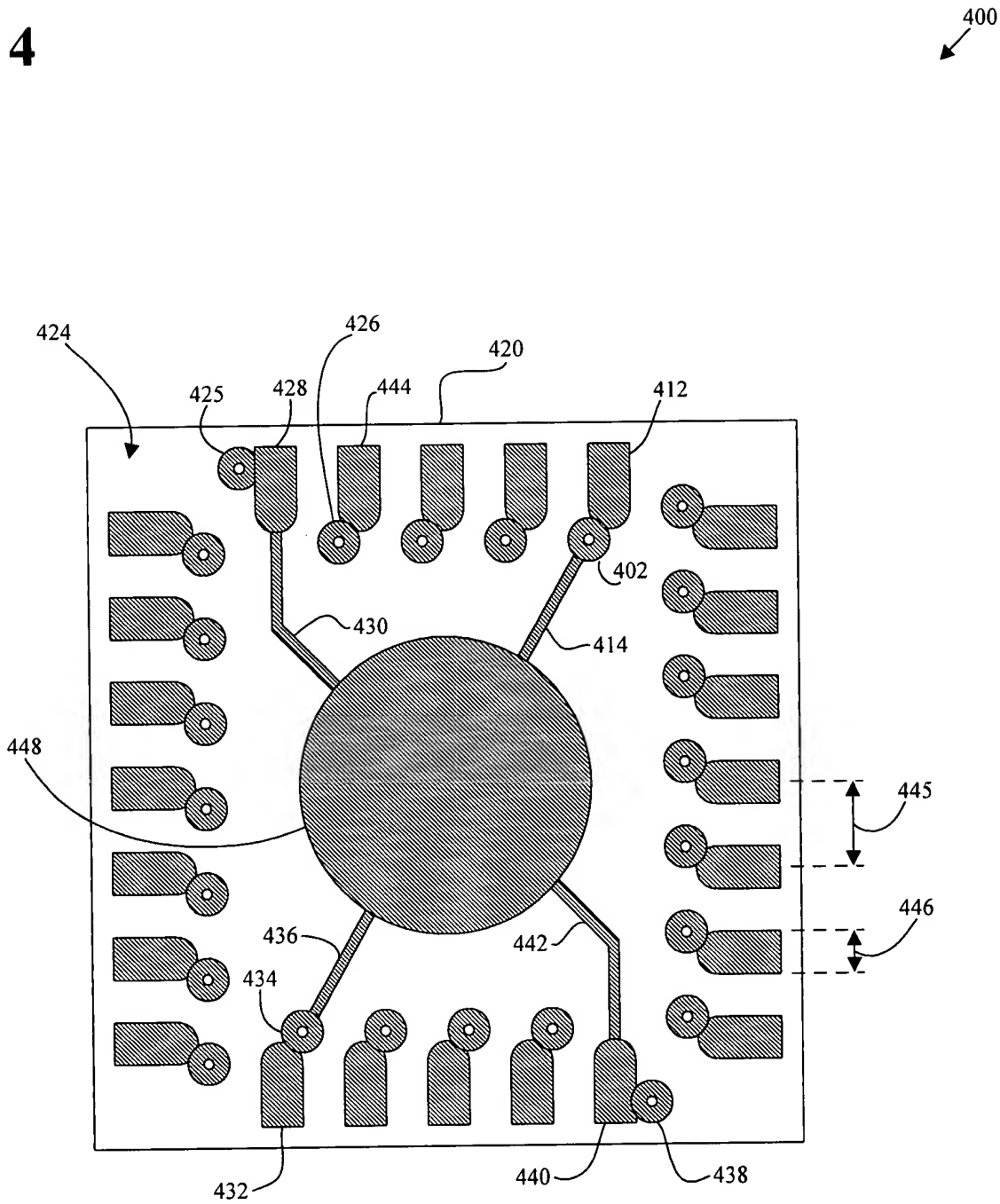
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Fig. 5

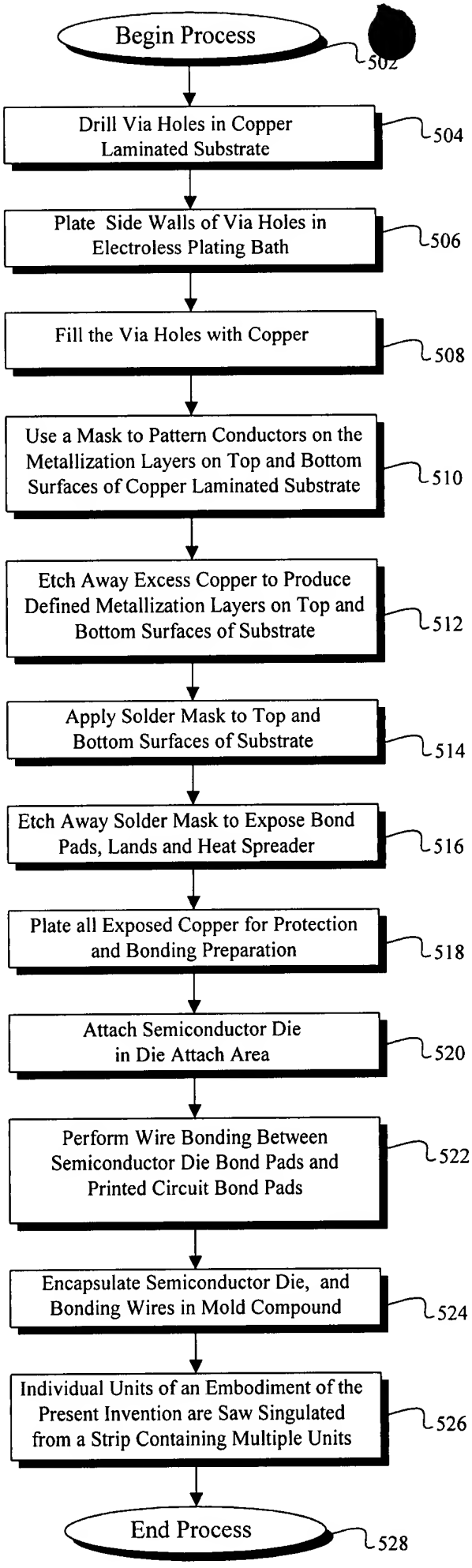

Begin Process
502
Drill Via Holes in Copper Laminated Substrate
504
Plate Side Walls of Via Holes in Electroless Plating Bath
506
Fill the Via Holes with Copper
508
Use a Mask to Pattern Conductors on the Metallization Layers on Top and Bottom Surfaces of Copper Laminated Substrate
510
Etch Away Excess Copper to Produce Defined Metallization Layers on Top and Bottom Surfaces of Substrate
512
Apply Solder Mask to Top and Bottom Surfaces of Substrate
514
Etch Away Solder Mask to Expose Bond Pads, Lands and Heat Spreader
516
Plate all Exposed Copper for Protection and Bonding Preparation
518
Attach Semiconductor Die in Die Attach Area
520
Perform Wire Bonding Between Semiconductor Die Bond Pads and Printed Circuit Bond Pads
522
Encapsulate Semiconductor Die, and Bonding Wires in Mold Compound
524
Individual Units of an Embodiment of the Present Invention are Saw Singulated from a Strip Containing Multiple Units
526
End Process
528

Fig. 6

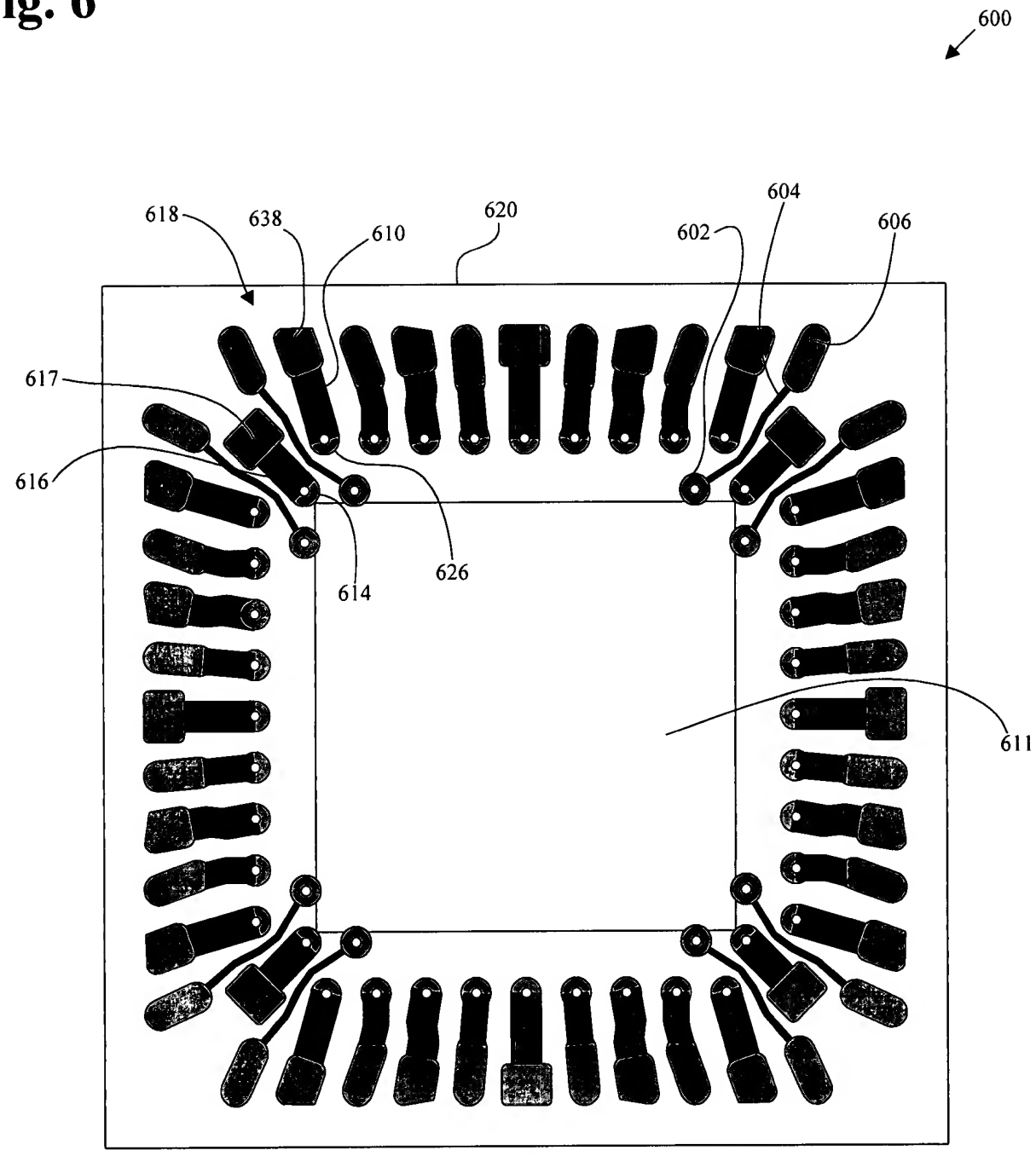
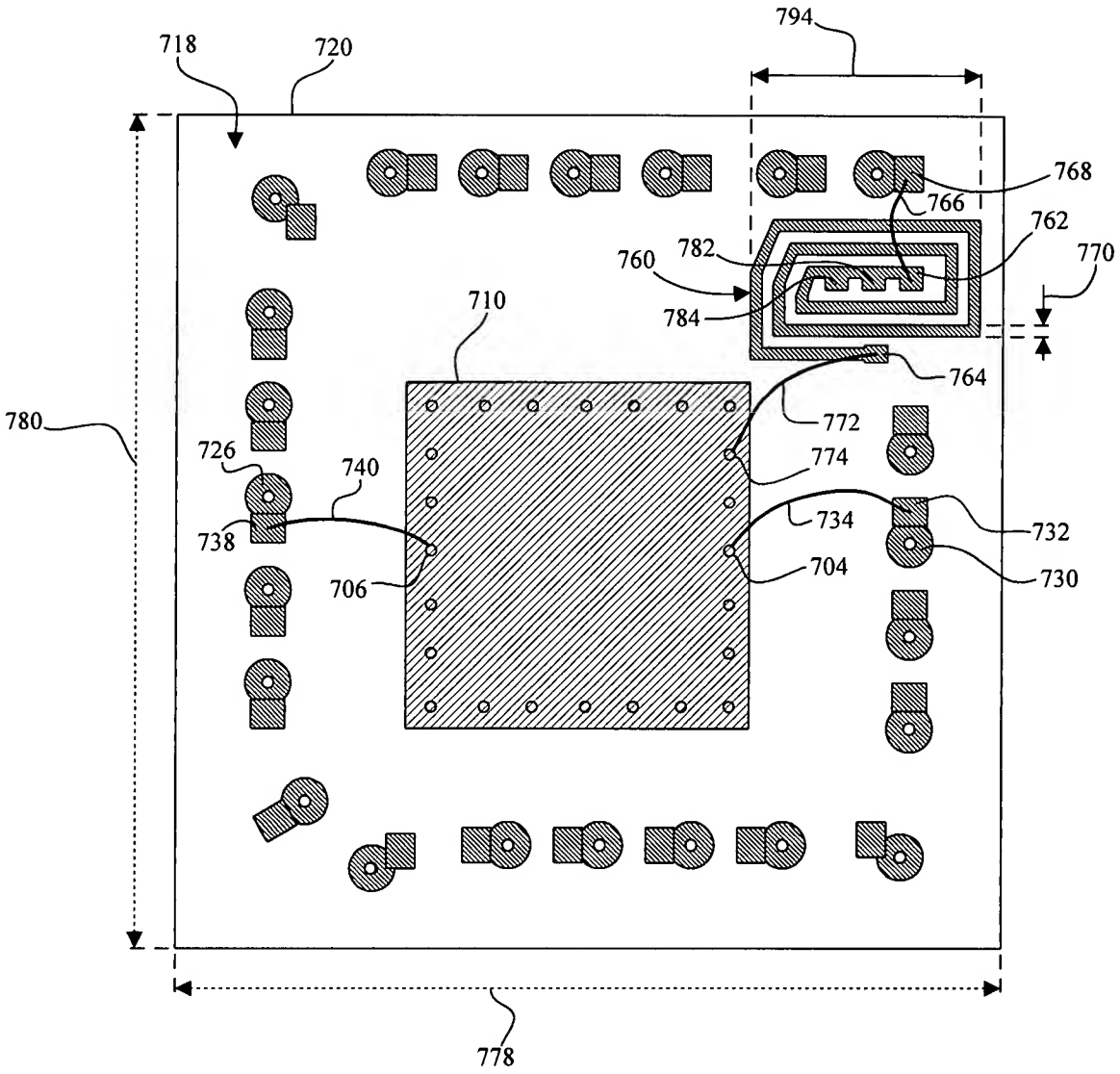


Fig. 7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SCANNED, # 12
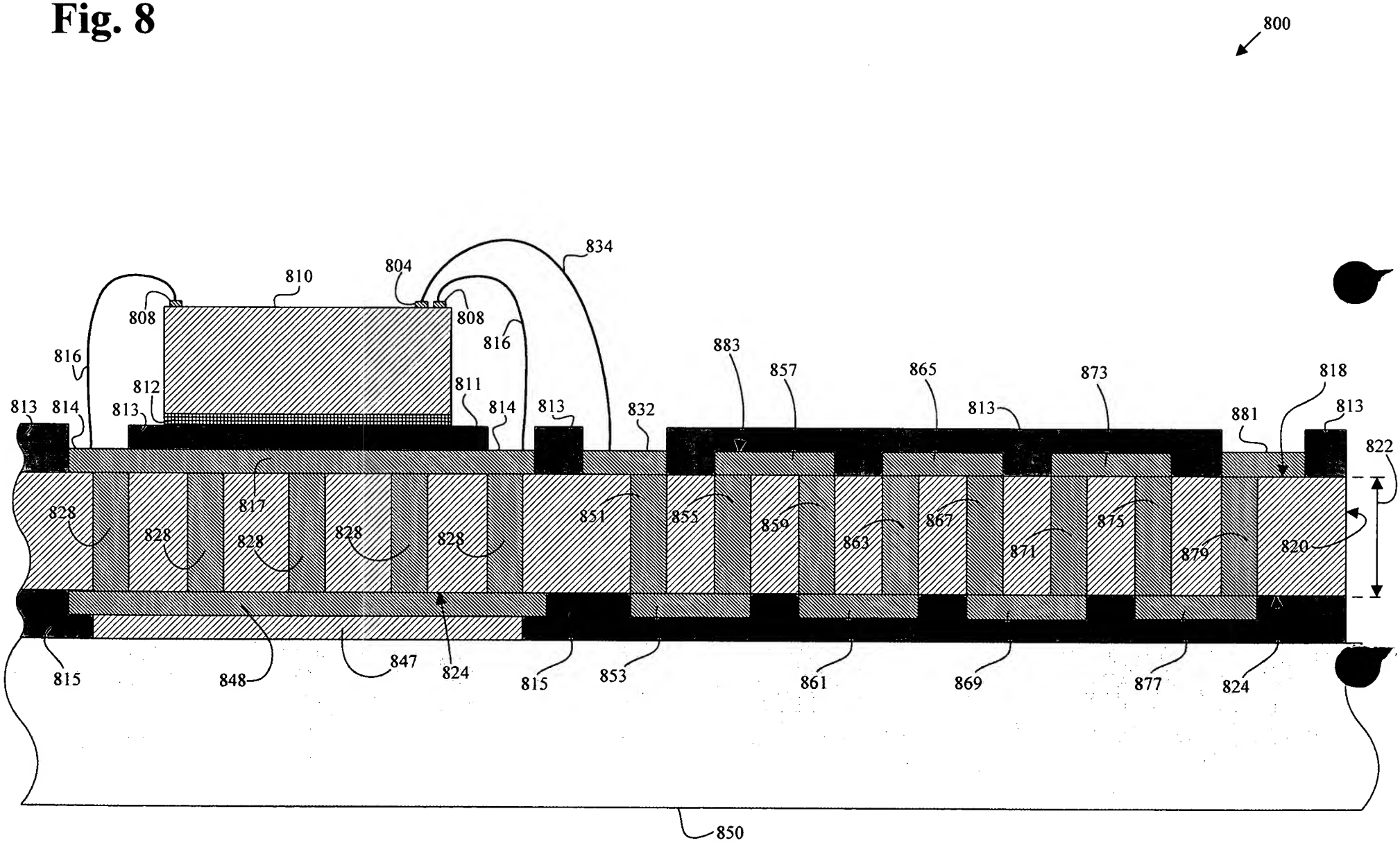
Fig. 8